Embodiment 1

[0029] FIG. **1** is a view showing a configuration of a semiconductor device according to Embodiment 1 of the present invention. The semiconductor device of Embodiment 1, which is shown in FIG. **1**, is composed by using a semiconductor substrate of silicon carbide and including a MOSFET and a diode. In FIG. **1**, on one of main surfaces of an N-type high-concentration (N^+-type) semiconductor substrate **101** of silicon carbide, a drift region **102** composed of an N-type low-concentration (N^--type) epitaxial layer made of silicon carbide is formed.

[0030] On one of main surfaces (that is, a front surface) of the drift region **102**, a P-type well region **103** and an N+-type source region **104** are formed. Moreover, there is formed a trench **105** with a depth penetrating the P-type well region **103** and the N+-type source region **104** and reaching the drift region **102**. In the drift region **102** immediately under the trench **105**, an anode region **106** is formed by selective introduction of impurities, and an upper surface of the anode region **106** forms a bottom surface of the trench **105**. This anode region **106** is formed of a P-type conductor in Embodiment 1, composes a PN junction-type diode on a junction surface with the N-type drift region, and functions as an anode of this diode.

[0031] On a side surface of the trench **105** and a bottom portion of the trench **105**, a gate insulating film **107** is formed so as to contact the drift region **102**, the well region **103** and the source region **104**. In a side surface of the trench, a gate electrode **108** is embedded while interposing the gate insulating film **107** therebetween. An interlayer insulating film **109** is formed on an upper surface of the gate electrode **108**, and coats the gate electrode **108**.

[0032] In the trench **105**, a contact hole **110** is formed so as to be surrounded by the gate electrode **108**. In the contact hole **110**, a source electrode **112** is formed while interposing therebetween an inner wall insulating film **111** which coats a side surface of the gate electrode **108**. The source electrode **112** is formed on the source region **104** and the interlayer insulating film **109**. This source electrode **112** connects the source region **104** and the anode region **106** to each other in an ohmic contact that is low in electrical resistance. The source electrode **112** and the gate electrode **108** are insulated from each other by the interlayer insulating film **109** and the inner wall insulating film **111**.

[0033] On other of the main surfaces (that is, a back surface) of the semiconductor substrate **101**, a drain electrode **113** is formed so as to be connected thereto in an ohmic contact that is low in electrical resistance.

[0034] Next, by using manufacturing process cross-sectional views shown in FIG. **2**A to FIG. **2**J, a description is made of a manufacturing method of the semiconductor device according to Embodiment 1.

[0035] First, in a process shown in FIG. **2**A, on such a one main surface of the N^+-type semiconductor substrate **101**, the drift region **102** composed of the N^--type epitaxial layer of silicon carbide is formed. Silicon carbide has some polytypes (crystal polymorphisms), and here, a description is made on the premise that the polytype is typical 4H. The semiconductor substrate **101** has a thickness ranging approximately from several ten to several hundred micrometers. The drift region **102** is formed, for example, with an impurity concentration ranging from 1E14 to 1E18 cm^{-3} and at a thickness ranging from several to several ten micrometers.

[0036] Next, in a process shown in FIG. **2**B, the P-type well region **103** and the N^+-type source region **104** are formed on the drift region **102** by ion implantation. A mask material may be formed on the drift region **102** by a process, which is shown below, in order to pattern an ion-implanted region. For example, a silicon oxidation film can be used as the mask material, and as a deposition method, a thermal CVD method and a plasma CVD method can be used.

[0037] Subsequently, resist is patterned (not shown) on the mask material. As a patterning method, a general photolithography method can be used. The mask material is selectively removed by etching by using the patterned resist as a mask. As an etching method, wet etching using hydrofluoric acid and dry etching such as reactive ion etching can be used.

[0038] After the mask material is selectively removed by etching, the resist is removed by oxygen plasma, sulfuric acid and the like. By using the patterned resist as a mask, P-type and N-type impurities are ion-implanted, and the P-type well region **103** and the N+-type source region **104** are formed. As the P-type impurities, for example, aluminum and boron can be used. As the N-type impurities, for example, nitrogen can be used. At this time, such ions are implanted in a state where the semiconductor substrate **101** is heated up to approximately 600° C., whereby a crystal defect can be suppressed from occurring in the implanted region.

[0039] After the ion implantation, the mask material is removed, for example, by the wet etching using hydrofluoric acid. Thereafter, the impurities thus ion-implanted are activated by performing heat treatment therefor. As a heat treatment temperature, a temperature of approximately 1700° C. can be used, and as an atmosphere, argon and nitrogen can be suitably used. This heat treatment process may be implemented after a process that is shown in FIG. **2**D and described later.

[0040] Next, in a process shown in FIG. **2**C, the trench **105** is formed in the drift region **102**. First, the mask material **201** is formed on the source region **104**. As the mask material **201**, an insulating film patterned in a similar way to the process previously shown in FIG. **2**B can be used. Subsequently, the trench **105** is formed by using the mask material **201** as a mask. As a method for forming the trench, the dry etching method is suitably used. The depth of the trench **105** is set at a depth penetrating the well region **103** and the source region **104** and reaching the drift region **102**.

[0041] Next, in a process shown in FIG. **2**D, the P-type anode region **106** is selectively formed in the drift region **102** immediately under the trench **105**. As a forming method of the anode region **106**, the ion implantation can be used. As a mask at the time of the ion implantation, the mask material **201** used in the process previously shown in FIG. **2**C can be used. In such a way, in the drift region **102** immediately under the trench **105**, the anode region **106** can be selectively formed in a self-alignment. Ion species for use in the ion implantation and a substrate temperature are similar to those in the process previously shown in FIG. **2**B, and accordingly, are omitted here.

[0042] Next, in a process shown in FIG. **2**E, on the upper surface of the anode region **106** (that is, the bottom surface of the trench **105**), on the side surface of the trench **105** and on the source region **104**, the gate insulating film **107** is deposited and formed, for example, at a thickness ranging approximately from 100 to 1000 Å. As the gate insulating film **107**, a silicon oxidation film can be suitably used, and as a deposi-